REMARKS

This is intended as a full and complete response to the Final Office Action dated September 26, 2005, having a shortened statutory period for response set to expire on December 26, 2005. Applicant submits this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-24 are pending in the application. Claims 1-24 remain pending following entry of this response. Claims 10 and 21 have been amended. New claim 25 has been added to recite aspects of the invention. Applicant submits that the amendments and new claims do not introduce new matter.

Claim Rejections - 35 U.S.C. § 102

Claims 1-4, 6, 10, 13-18 and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by *Lehmann* (US 6,798,272). Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). As described below, *Lehmann* does not disclose "each and every element as set forth in the claim".

Description of the Cited Art

Lehmann discloses a shift register for sequential fuse latch operation. The sequential fuse latch device comprises a plurality of fuse latches, wherein each fuse latch is a data storage element, and a shift register comprising a plurality of pointer latches, wherein each pointer latch is connected to at least one fuse latch, and wherein the shift register controls a sequential operation of the plurality of fuse latches.

Lehmann describes a fuse latch device, as shown in Fig. 2, wherein a number of fuse latches 200 are connected to current power supply lines 208 and 209. The power

supply connections 210 and 211 exhibit an internal resistance 212 and 213. Each fuse latch 200 comprises a data storage element and a fuse and has a separate input signal 201, which controls the precharge operation and a separate input signal 202, which controls the read operation. The signals 201 and 202 are generated by another group of pointer latches 214, wherein for each fuse latch 200, a second or pointer latch 214 exists. In the configuration shown in Fig. 2 of *Lehmann*, a fuse latch 200 receives the read signal 202 from one of the latches 214 and the precharge signal 201 from another latch 214. The latches 214 share a common clock signal 216 and a common initialize signal 218. Furthermore, the latches 214 are connected together by signals 215 to create a shift register (column 3, lines 57 - 60). The latches 214 store a signal value indicative as to which fuse latch 200 has to be precharged or read (column 3, lines 60 - 62).

The Cited Reference Does not Teach All Elements of the Claimed Invention

In light of the description above, *Lehmann* does not teach all elements of the claimed invention.

For example, Claim 1 describes a shift register circuit comprising a plurality of stages, each comprising a data latch circuit for storing a bit of data, and a pointer latch circuit for storing a bit of pointer information. In contrast thereto, *Lehmann* only discloses that for each fuse latch (Item 200), a second pointer latch (Item 214) exists (see Fig. 2 and column 3, lines 53 to 55). *Lehmann* does not disclose that fuse latch (Item 200) and pointer latch (Item 214) form a stage of the shift register. On the contrary, *Lehmann* clearly discloses that the shift register only comprises the pointer latches (Item 214) (column 2, lines 18 to 19), but not fuse latches. Furthermore, the fuse latches (Item 200) can not be part of the shift register, as only the pointer latches (Item 214) are connected together by signals (Item 215) to create a shift register (column 3. lines 57 - 60 and Fig. 6). Thus, the fuse latches (Item 200) are not part of the shift register (column 2. lines 20 to 22), but merely receive control signals from the pointer latches (Item by precharge signal 201 and read signal 202). Accordingly,

Lehmann does not disclose that a fuse latch (Item 200) and a pointer latch (Item 214) form a stage of the shift register.

Furthermore, with respect to Claim 1, the claim describes a transfer circuitry for serially transferring bits of data presented at the data input and to be stored in the data latch circuits through the plurality of stages during a first mode of operation. As stated in the claim, a stage of the serial shift register comprises a pointer latch circuit and a data latch circuit. Thus, the bits of data are serially shifted through the pointer latch circuit and the data latch circuit of the plurality of stages during a first mode of operation. In contrast, *Lehmann* describes a shift register, wherein, as disclosed in Fig. 2 and column 3, lines 55 to 57, a fuse latch (Item 200) receives the read signal (Item 202) from one of the pointer latches (Item 214) and the precharge signal (Item 201) from another pointer latch (Item 214). Thus, *Lehmann* does not disclose that bits of data (Item 215) are serially transferred, *e.g.* as a signal (Item 201 or 202), to the fuse latch (Item 200) nor that the bits of data (Item 215) are to be stored in the fuse latch (Item 200). Accordingly, *Lehmann* does not describe a transfer circuitry for serially transferring bits of data presented at the data input and to be stored in the data latch circuits through the plurality of stages during a first mode of operation.

Therefore, *Lehmann* does not teach the claimed subject matter. Accordingly, Applicant believes the claims are in condition for allowance, and withdrawal of this rejection is respectfully requested.

Allowable Subject Matter

Claims 5, 7-9, 11, 12, 14, 15, 19, 20 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

For reasons described above, however, Applicant believes the base claims from which these claims depend are allowable. Accordingly, Applicant submits these claims are also allowable and request withdrawal of this objection.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted,

Gero G. McClellan
Registration No. 44,227
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)